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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/161,405	09/28/1998	HIRAKU KOZUKA	862.2480	7603

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EXAMINER	
WHIPKEY, JASON T	

ART UNIT	PAPER NUMBER
2612	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/161,405	KOZUKA, HIRAKU	
	Examiner	Art Unit	
	Jason T. Whipkey	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 December 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8,11,14 and 33-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8,11,14,33-35,37 and 38* is/are rejected.

7)☒ Claim(s) *36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 September 1998* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *17 December 2002* is: a)☒ approved b)☐ disapproved by the Examiner

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed December 17, 2002, with respect to claims 8, 11, 14, and 33-38 have been considered but are moot in view of the new ground of rejection.

Drawings

2. The proposed drawing correction filed on December 17, 2002, has been approved. A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

Specification

3. The new title and the changes to the specification have been approved and the corresponding objections withdrawn.

Claim Objections

4. Since claims 1 and 26 have been cancelled, the examiner's objections to them are now moot. No objections to the claims remain.

Claim Rejections - 35 USC § 101

5. Since claims 1-4 have been cancelled, the corresponding rejections under 35 U.S.C. 101 are now moot. No rejections to the claims under 35 U.S.C. 101 remain.

Claim Rejections - 35 USC § 112

6. Since claims 1-4, 6, 7, 9, 10, and 12-13 have been cancelled, the corresponding rejections under 35 U.S.C. 112 are now moot. No rejections to the claims under 35 U.S.C. 112 remain.

Double Patenting

7. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

8. Claims 33 and 38 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 12 of U.S. Patent No. 6,002,287. Although the conflicting claims are not identical, they are not patentably distinct from each other.

Claim 12 in the issued patent does not specifically claim that each of the integrated circuit chips has a plurality of photoelectric conversion circuits. However, it does claim that the chips have "a plurality of signal sources". Official Notice is taken that photoelectric conversion circuits are commonly used to provide a signal. Since claim 12 in the issued patent does not claim any specific type of signal source, it would have been obvious at the time of invention to use any signal source, such as photoelectric conversion circuits.

Claim 12 in the issued patent also does not specifically claim that each of the signal sources shares a common output line. However, it does claim that each chip has "an output terminal for outputting output signals from said signal sources". Official Notice is taken that signals from multiple sources often share a common output line. An advantage to doing so is that less wiring is required within the chip, reducing its size. For this reason, it would have been obvious at the time of invention to have each of the signal sources share a common output line between them and the chip's output terminal.

Claim 12 in the issued patent also does not specifically claim that the correct circuit receives a noise signal from the integrated circuit chips. However, it does claim that the correct circuit is used "for reducing a difference among offset voltages of the

output signals from said integrated circuit chips". Official Notice is taken that correlated double sampling circuits are often used to reduce noise (an offset) in signals from photosensors by subtracting the noise — which is obtained from the photosensor itself — from the image signal. Since noise varies among photoelectric conversion devices, an advantage to using a noise signal read directly from a photoelectric conversion device to reduce said device's noise is that the device itself is the most accurate location from which the noise may be measured. For this reason, it would have been obvious at the time of invention to have the correct circuit obtain its offset from the integrated circuit chips.

Claim 38 in the instant application is a method claim, while claim 12 in the issued patent is an apparatus claim. Although the issued patent does not explicitly claim that the correct circuit is driven to compensate for noise present in the signals read from the chips, it is inherent that the apparatus in claim 12 performs this function, as it is "for reducing a difference among offset voltages of the output signals from said integrated circuit chips ... [and] is input with outputs of all of the other integrated circuit chips, whereby the correct output signal is obtained" (lines 5-10).

Under the principles of inherency, if a prior art device necessarily performs the method claimed in its normal and usual operation, then the prior art device anticipates the method. See MPEP §2112.02.

9. Claims 33 and 38 are directed to an invention not patentably distinct from claim 12 of commonly assigned U.S. Patent No. 6,002,287. See the explanation above.

The U.S. Patent and Trademark Office normally will not institute an interference between applications or a patent and an application of common ownership (see MPEP § 2302). Commonly assigned U.S. Patent No. 6,002,287, discussed above, would form the basis for a rejection of the noted claims under 35 U.S.C. 103(a) if the commonly assigned case qualifies as prior art under 35 U.S.C. 102(f) or (g) and the conflicting inventions were not commonly owned at the time the invention in this application was made. In order for the examiner to resolve this issue, the assignee is required under 37 CFR 1.78(c) and 35 U.S.C. 132 to either show that the conflicting inventions were commonly owned at the time the invention in this application was made or to name the prior inventor of the conflicting subject matter. **Failure to comply with this requirement will result in a holding of abandonment of the application.**

A showing that the inventions were commonly owned at the time the invention in this application was made will preclude a rejection under 35 U.S.C. 103(a) based upon the commonly assigned case as a reference under 35 U.S.C. 102(f) or (g), or 35 U.S.C. 102(e) for applications filed on or after November 29, 1999.

Claim Rejections - 35 USC § 103

10. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

11. All of the rejections below over Nakamura refer to U.S. Patent No. 5,321,528.

12. Claims 33-35, 37, and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Rahmouni.

Regarding claims 33 and 38, Nakamura discloses an image sensor consisting of multiple sensor chips that are "aligned" (column 2, line 66, through column 3, line 4), indicating they are mounted on a base. Each chip — 1-1 in Figure 1, for example — has an output bus (unlabeled) connecting the drains of transistors 6-1-1, 6-1-2, etc., which are connected to photoconversion cells 2-1-1, 2-1-2, etc. The output bus in each chip is used to output light signal voltage V2 (column 3, lines 52-55) and noise signal voltage V1 (column 3, lines 36-41). Amplifiers 9-1 *et al.* output the signal from the output bus of each chip.

An amplifier circuit, consisting of parts 33-39 shown in Figure 3, receives the output of an inter-chip bus. Buffer amplifier 33 receives the both the noise signal V1 (column 4, lines 3-8) and the light signal V2 (column 4, lines 16-20) from the bus. Capacitor 35 receives these signals and finds the difference (column 4, lines 16-30). Components 33-39 comprise a correction circuit 140 (column 5, lines 11-16), and correction circuit 140 is part of a printed circuit board (column 5, lines 56-58).

Nakamura is silent with regard to including the amplifier circuit on the base with the sensor chips.

Rahmouni discloses a mounting apparatus for a charge coupled photo device. The CCPD shown in Figure 4 is in chip form (column 1, lines 55-58) and is mounted directly on a printed circuit board (column 4, lines 56-57). The PCB "also contains certain signal conditioning and processing circuitry" (column 5, lines 10-15).

As stated in column 5, lines 12-15, the advantage to mounting a chip holding an image pickup device to a printed circuit board holding processing circuitry is that placing the chip as close as possible to the circuitry "avoid[s] undesired electromagnetic effects and obtain[s] the desired amplification of the CCPD signals in the most efficient manner." For this reason, it would have been obvious at the time of invention to have Nakamura include his image processing circuitry on the board on which the chips are attached.

Regarding claim 34, Nakamura discloses a differential circuit (capacitor 35) as described above. Additionally, capacitor 35 is part of a clamping circuit consisting of parts 35-38. The clamping circuit clamps the signal using clamping voltage VC from clamped voltage source 38 (column 4, lines 11-12).

Regarding claim 35, the chip is reset via reset terminal 24 (column 3, lines 39-40). After the inter-chip bus is reset, clamping circuit 35-38 clamps the reset state (column 4, lines 5-12).

Regarding claim 37, Nakamura shows that capacitor 35 is part of a clamping circuit consisting of parts 35-38. The clamping circuit clamps the signal using clamping voltage VC from clamped voltage source 38 (column 4, lines 11-12).

13. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Rahmouni and further in view of Surisawa.

Claim 8 may be treated like claim 33. However, both Nakamura and Rahmouni are silent with regard to using a power supply voltage with the photosensor chips that is lower than the power supply voltage supplied to the processing means.

Surisawa discloses an image sensor on a substrate 1 (Figure 10A). The voltage V_{sub} supplied to the substrate is larger than the voltage V_D supplied to the image sensor (column 13, lines 6-8). The advantage to having separate power supplies is that the appropriate voltage may be supplied to each component without excess, which saves power. For this reason, it would have been obvious to have separate power supplies for the chips and the substrate.

14. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Rahmouni and further in view of Hamasaki.

Claim 11 may be treated like claim 33. However, Nakamura and Rahmouni are both silent with regard to isolating the ground wiring for the photosensor chips and the processing circuitry.

Hamasaki discloses an image pickup device on a substrate 72 (Figure 4). Output section 78 is also included on substrate 72. Grounding wiring 80 grounds the imaging area (column 6, lines 33-42). Grounding wiring 88 grounds output section 78 (column 6, lines 51-56). As stated in column 6, line 68, through column 7, line 7, this prevents output section 78 from affecting the sensing section. For this reason, it would have been obvious for Nakamura's system to include separate ground wiring for the photosensor chips and the processing circuitry.

15. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Rahmouni and further in view of Surisawa and Hamasaki.

Claim 14 may be treated like claim 8. However, Nakamura, Rahmouni, and Surisawa are all silent with regard to isolating the ground wiring for the photosensor chips and the processing circuitry.

Hamasaki discloses an image pickup device on a substrate 72 (Figure 4). Output section 78 is also included on substrate 72. Grounding wiring 80 grounds the imaging area (column 6, lines 33-42). Grounding wiring 88 grounds output section 78 (column 6, lines 51-56). As stated in column 6, line 68, through column 7, line 7, this prevents output section 78 from affecting the sensing section. For this reason, it would have been obvious for Nakamura's system to include separate ground wiring for the photosensor chips and the processing circuitry.

Allowable Subject Matter

16. Claim 36 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

No prior art could be located that teaches or fairly suggests a noise compensation circuit with a plurality of serially connected clamp circuits connected to the output of an image sensor.

Conclusion

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

18. Applicant's amendment necessitated the new ground of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason T. Whipkey, whose telephone number is (703) 305-1819. The examiner can normally be reached Monday through Friday from 9 A.M. to 6:30 P.M. eastern standard time, alternating Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy R. Garber, can be reached on (703) 305-4929. The fax phone number for the organization where this application or proceeding is assigned are (703) 872-9314 for both regular communication and After Final communication.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office, whose telephone number is (703) 306-0377.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to (703) 872-9314 for either formal or informal communications intended for entry. (For informal or draft communications, please label **"PROPOSED"** or **"DRAFT"**.)

Hand-delivered responses should be brought to the sixth floor receptionist of Crystal Park II, 2121 Crystal Drive in Arlington, Virginia.

JTW

JTW
February 24, 2003

WENDY R. GARBER
SUPERVISORY PATENT EXAMINER
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